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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,530	11/24/2003	David Lewis	174/304	8666
36981 75	590 03/18/2005		EXAM	INER
FISH & NEAVE IP GROUP			TRAN, ANH Q	
ROPES & GRAY LLP				
1251 AVENUE OF THE AMERICAS FL C3			ART UNIT	PAPER NUMBER
NEW YORK, NY 10020-1105			2819	

DATE MAILED: 03/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
<b></b>	10/723,530	LEWIS, DAVID				
Office Action Summary	Examiner	Art Unit				
	Anh Q. Tran	2819				
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with th	he correspondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply If NO period for reply is specified above, the maximum statutory period w  - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a reply by within the statutory minimum of thirty (30 vill apply and will expire SIX (6) MONTHS cause the application to become ABAND	be timely filed ) days will be considered timely. from the mailing date of this communication. ONED (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) filed on 24 No.	ovember 2003.					
2a) ☐ This action is <b>FINAL</b> . 2b) ☑ This	This action is <b>FINAL</b> . 2b)⊠ This action is non-final.					
• • • • • • • • • • • • • • • • • • • •	3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practice under E	x parte Quayle, 1935 C.D. 11	, 453 O.G. 213.				
Disposition of Claims						
4)⊠ Claim(s) <u>1-37</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6) Claim(s) <u>1,3,9,16-26,29,30 and 32-37</u> is/are rej						
7) Claim(s) <u>2,4-8,10-15,27,28 and 31</u> is/are object						
8) Claim(s) are subject to restriction and/or	r election requirement.	÷				
Application Papers		•				
9) The specification is objected to by the Examine	r. "					
10)⊠ The drawing(s) filed on 24 November 2003 is/a	re: a)⊠ accepted or b)□ ob	jected to by the Examiner.				
Applicant may not request that any objection to the	drawing(s) be held in abeyance.	See 37 CFR 1.85(a).				
Replacement drawing sheet(s) including the correct	ion is required if the drawing(s) is	s objected to. See 37 CFR 1.121(d).				
11) The oath or declaration is objected to by the Ex	aminer. Note the attached Of	fice Action or form PTO-152.				
Priority under 35 U.S.C. § 119						
12) ☐ Acknowledgment is made of a claim for foreign a) ☐ All b) ☐ Some * c) ☐ None of:  1. ☐ Certified copies of the priority documents 2. ☐ Certified copies of the priority documents 3. ☐ Copies of the certified copies of the priority	s have been received. s have been received in Appli rity documents have been rec	ication No				
application from the International Bureau	- · · · ·	aired				
* See the attached detailed Office action for a list	oi trie certified copies not rec	eiveu.				
American (1)						
Attachment(s)  1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)	5) D Notice of Inform	mary (PTO-413) ail Date nal Patent Application (PTO-152)				
Paper No(s)/Mail Date 11/24/03.	6)  Other:	•				

Application/Control Number: 10/723,530 Page 2

Art Unit: 2819

#### **DETAILED ACTION**

### Claim Rejections - 35 USC § 112

- 1. The following is a quotation of the second paragraph of 35 U.S.C. 112:
  - The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 2. Claim 32 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Both the first-mentioned stage and the second-mentioned stage have third stage that is both a source stage and a destination stage. The recites limitations in the claim are very confusing and vague. Clarification is requires.
- 3. claims 33-37 are rejected as dependent on claim 32.

## Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 1, 3, 9, 16-18, 19-20, 25-26, 29-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Young et al (6,107,827).

#### Young shows:

1. Logic module circuitry comprising: combinational logic circuitry having at least first (J, H), second (F5A, F6A), and third stages (MJ, MH); and XOR circuitry (SH, SJ)

Application/Control Number: 10/723,530 Page 3

Art Unit: 2819

interposed between two of the stages for logically combining a carry in signal (CIN1) with at least one combinational signal (H or J output) in the combinational logic circuitry.

- 3. the circuitry defined in claim 1 further comprising: circuitry for producing a carry out signal (CJ) from the carry in signal and combinational signals in the combinational logic circuitry (MJ or MH).
- 9. The circuitry defined in claim 1 wherein the XOR circuitry is interposed between the second and third stages.
- 16-18. The circuitry defined claim 1 wherein the first and second stages are programmable to produce an output signal that is usable in forming an arithmetic sum of first and second stage input signals, difference between first and second stage input signals or product of first and second stage input signals (inherent limitations, since function generators J, H, G, F are programmable to do these functions).
- 19. The circuitry defined in claim 18 wherein the third stage (MJ, MH) and the XOR circuitry are operable to form the arithmetic sum of the output signal, a third stage input signal (output O from H), and a carry in signal (CIN1).
- 20. A programmable logic device comprising logic module circuitry as defined in claim 1.

The apparatus described above is applicable to the method claims 25-26, 29-30.

# Claim Rejections - 35 USC § 103

3. Claims 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Young et al (6,107,827) in view of Park et al (6,359,468).

Application/Control Number: 10/723,530

Art Unit: 2819

Young discloses the claimed invention except for a memory, processing circuitry, and programmable logic device mounted on a printed circuit board. Park discloses a memory, processing circuitry, and programmable logic device mounted on a printed circuit board. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the programmable logic device of Young in a digital processing system of Park, in order to provide wide variety of applications where the advantage of using programmable logic device.

#### Allowable Subject Matter

4. Claims 2, 4-8, 10-15, 27-28, 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

ANH Q.TRAN PRIMARY EXAMINER

1/alon

Page 4